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The effect of parasitic boron doping on P-type piezoresistors

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Abstract

Absolute piezoresistive pressure sensors often use direct wafer bonding of SOI with the etched bulk silicon to provide us with sensitive membranes and sealed cavities. The advantage of such a process is that we can easily obtain a thin, monocrystalline silicon membrane with controlled thickness and a vacuum sealed cavity. However, few works have been reported on the electrical quality of this N-type membrane and its influence on performance of the P-type gauges. The problem of parasitic Boron appearance at the Si/SiO₂ interface was only recently shown in BESOI wafers, but it becomes much more significant when creating the component at the bottom side of the device layer, like in the case of an absolute piezoresistive pressure sensor.

Keywords: SOI interface; Pressure sensors; Parasitic doping

1. Introduction

The direct wafer bonding of the SOI wafers with the etched bulk silicon is a known technique that is used in the sealed cavities formation for many applications including absolute pressure sensors or accelerometers [1, 2]. As the main part of such a mechanical system is the membrane, there was a lot of work in the field concerning the quality of the bonding process [3] in order to obtain good mechanical parameters of the designed system.

Nevertheless, in the case of piezoresistive pressure sensors, if we want to use such a membrane to fabricate the piezoresistive strain gauges by ion implantation technique, we must create the device on the bottom side of the device layer of the SOI wafer that forms the membrane. It causes that the device layer should not only possess good mechanical, but also electrical properties like initial doping level or its uniformity. Moreover, the bonding process itself should be analyzed in order to verify if there is no impact of the bonded materials on the electrical quality of the created membrane.

However, few works have been reported on the electrical quality of the N-type membrane and its influence on performance of P-type strain gauges that are used due to the higher coefficient of piezoresistivity. One of such a problem was the parasitic Boron appearance at the Si/SiO₂ interface that was only recently shown in BESOI wafers [4].

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2. Test structure

The process flow we used to fabricate our pressure sensor is schematically presented on a Fig. 1. It consists of the cavity formation on a bulk silicon wafer by etching the about 1.3 μm thick thermal oxide layer (Fig. 1a). Such a technique was used as the oxide layer provides us with the excellent electrical isolation from the substrate and all SOI device layer related advantages may be kept. The SOI wafer (Fig. 1b) is then bonded to the first one using the direct bonding SiO_2/Si technique creating the sandwich structure with the SOI wafer as the very thick membrane (Fig. 1c). Before the first phase of the bonding process, the two wafers are cleaned in order to make two surfaces hydrophilic. The standard solution that is used for such a purpose is a warm SC-1 (1:1:5 $\text{NH}_3:\text{H}_2\text{O}_2:\text{H}_2\text{O}$). Just after the cleaning procedure the wafer are put into bonding machine (in our case it was AML-AWB) and then put into intimate contact using the force of 2000N. In order to obtain necessary bond strength, the bonded pair is then annealed at 1150°C for 2h. Then, the top, bulk silicon from the SOI wafer is removed in two stages. First, the mechanical grinding is used in order to obtain about 50 μm thick membrane. At the end of such a process, the membrane is too fragile to continue mechanical grinding and the rest of the bulk silicon is etched in KOH solution (Fig. 1d). As a last step, the buried oxide layer is removed by the wet etching with HF solution (Fig. 1e). Such a structure may serve us for further processing in order to fabricate the absolute pressure sensor.

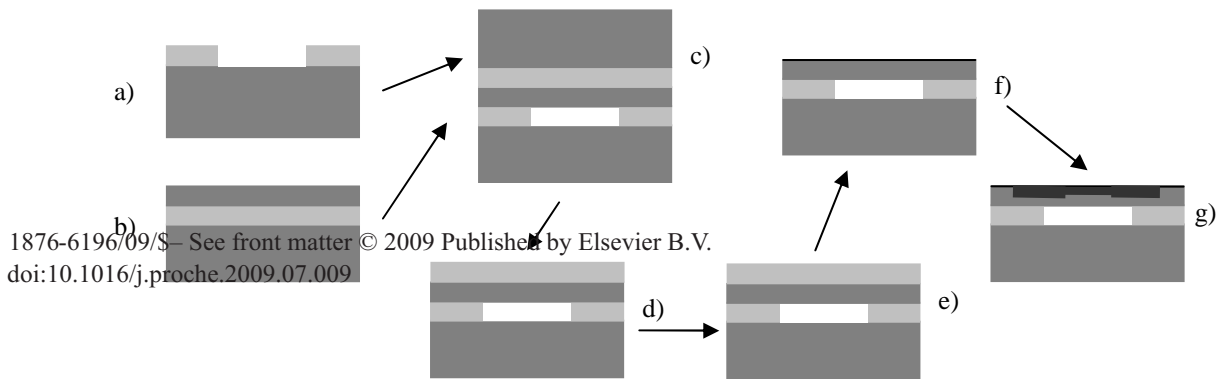


Fig. 1. Process flow of the sealed cavity based absolute piezoresistive pressure sensor.

Finally, the structure is further processed as a normal Si wafer in order to create the “electronic” components. The thin (400Å) screening oxide layer is thermally grown (Fig. 1f) and moderately doped strain gauges (P+) are fabricated by the Boron implantation followed by the high temperature annealing (Fig. 1g). As in order to obtain the good ohmic contact between metallic interconnections and strain gauges the necessary doping concentration is needed (approximately in order of 10^{19} at/cm³), the highly doped interconnections (P++) were created using the same process as for the strain gauges but with much higher implantation dose. The characteristics of the final test structure which was used for the electrical measurements are shown on a Fig 2.

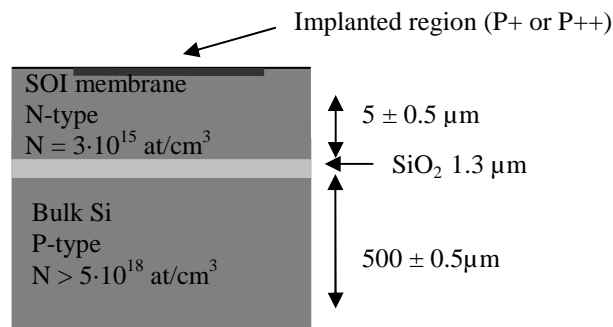


Fig. 2. Characteristics of the test structure used for the electrical measurements.

3. Measurements

Electrical measurements performed using the standard on-wafer testing facility including probestation, showed that the gauges resistance value was about ten times lower than it was predicted. Such a result forced us to run the detailed investigation about the possible reason of such a behaviour.

We decided to perform the SIMS analysis of the P+ and P++ layers in order to determine obtained doping profiles as they are fully responsible for the resistance value. The result of such an analysis for the strain gauge (Fig. 3a) and both (P+ and P++) layers (Fig. 3b) are shown below.

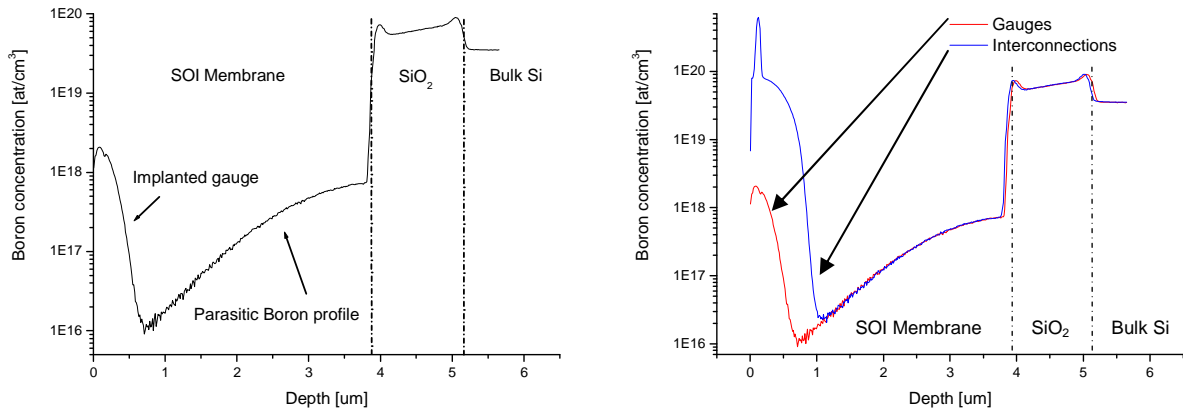


Fig. 3. (a) The SIMS profile representing the Boron concentration in the function of the depth; (b) The comparison of both P+ and P++ profiles proving that the parasitic Boron concentration comes from the oxide layer.

What we may clearly observe is that there is a parasitic P-type layer formed by Boron distribution in the membrane bottom side, which causes short-circuits. As for the bulk layer, that was thermally oxidized, the highly doped (about $5 \cdot 10^{19}$ at/cm³) silicon wafer was used, such an effect may be explained by the strong Boron diffusion from the bulk Si wafer through the very thick (about 1.3 μm) SiO₂ layer during the long thermal annealing performed after the bonding. Going further, as the gauges are fabricated at the bottom side of the SOI device layer, we decided to perform another SIMS analysis of the unimplanted area what is shown on Fig 4a.

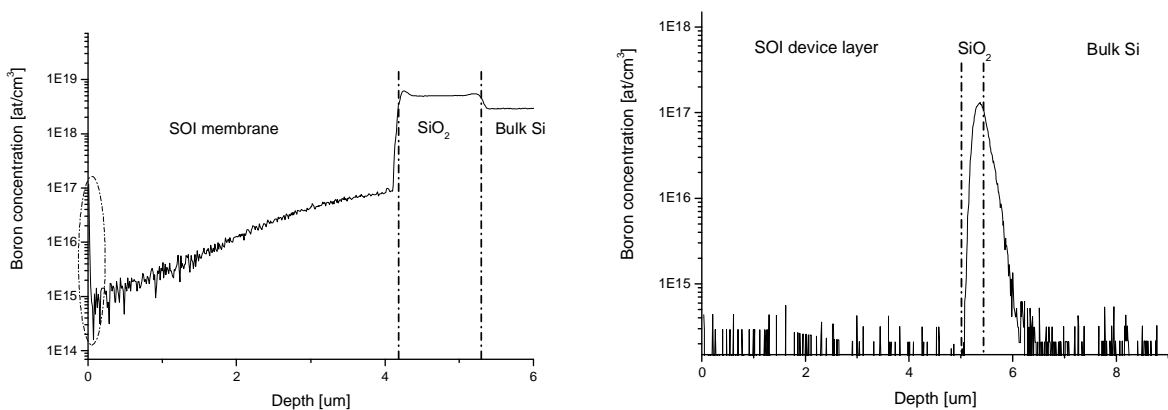


Fig. 4. (a) The SIMS profile of the unimplanted wafer area with a clear parasitic Boron profile and a thin zone at the surface containing the high Boron concentration of about $5 \cdot 10^{16}$ at/cm³; (b) The SIMS profile of the N-type unprocessed wafer with the clear, P-type parasitic doping at the SiO₂/Si interface.

As a result, not only did we observe the same phenomenon of parasitic Boron profile as for the doped zones, but also the Boron concentration reaching $5 \cdot 10^{16}$ at/cm³ in the thin layer (about 50 nm), at the membrane surface was found. Thus, the P-type layer which short-circuited all the gauges on a N-type membrane may also exist. Therefore, we verified the intrinsic quality of a SOI wafer by performing SIMS analysis on the unprocessed wafer (Fig. 4b). The quite high concentration of Boron in the buried oxide ($1 \cdot 10^{17}$ at/cm³) was found so it seems, that the Si/SiO₂ interface might be considered as a parasitic source of Boron which diffused into device layer during the post-bonding thermal annealing. The wafer used was delivered by the ULTRASIL® corporation and the Boron existence in the P-type layer was also recently reported [4]. According to some earlier reports [5] presenting such a problem due to the industrial savings on the double oxidation of both bonded wafers used for the SOI fabrication, it seems that still some efforts have to be made prior to the fabrication steps in order to choose the correct wafer. For a comparison, we performed a similar analysis with the wafer from the different vendor where we created highly doped P++ layer what is shown on Fig. 5. As one can see, no Boron is found at the SiO₂/Si interface.

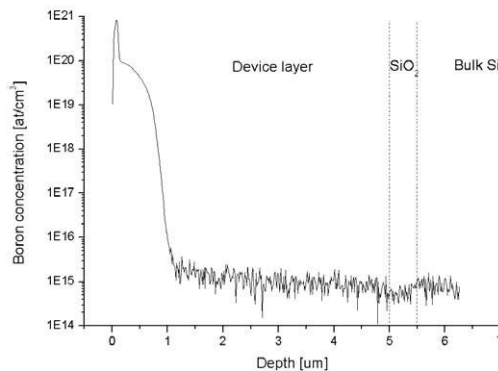


Fig. 5. The SIMS profile of another SOI wafer with created highly doped interconnections zone. No Boron is found at the SiO₂/Si interface.

4. Conclusions

In summary, the interface quality between silicon and buried oxide in SOI wafers is crucial for the fabrication of absolute piezoresistive pressure sensors, as well as the proper substrate wafer choice. As we could see, even the 1.3 μm thick layer can not be treated as a good barrier that stops Boron diffusion from the highly doped Si wafer. Thus, the high resistivity wafers should be rather used for similar process. Moreover, we confirmed the recently published problem of the Boron contamination in the N-type SOI wafers. As a solution to this problem, we propose to remove the thin Boron contaminated surface layer just before the gauge fabrication by the low temperature chemical wafer thinning, as an alternative to the most common method, based on the high temperature oxidation which may cause additional Boron diffusion inside the membrane.

References

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